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EXAMINER	
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JIMMIES EARL DEWITT JR.,
FRANK ELIOT LEVINE,
CHRISTOPHER MICHAEL RICHARDSON,
and ROBERT JOHN URQUHART

Appeal 2009-005534
Application 10/757,186
Technology Center 2100

Before JOSEPH L. DIXON, HOWARD B. BLANKENSHIP, and
JEAN R. HOMERE, *Administrative Patent Judges.*

BLANKENSHIP, *Administrative Patent Judge.*

DECISION ON APPEAL[1]

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, or for filing a request for rehearing, as recited in 37 C.F.R. § 41.52, begins to run from the "MAIL DATE" (paper delivery mode) or the "NOTIFICATION DATE" (electronic delivery mode) shown on the PTOL-90A cover letter attached to this decision.

STATEMENT OF THE CASE

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 1-23, which are all the claims remaining in the application. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm-in-part.

Invention

Appellants' invention relates to performance monitoring, and in particular to qualifying events by types of interrupt when interrupt occurs in the processor of a data processing system. Abstract.

Representative Claim

1. A data processing system for qualifying events when an interrupt occurs, comprising:

an interrupt unit control register for indicating an interrupt type selected to be monitored;

an interrupt unit, responsive to an interrupt occurring during code execution, for determining whether the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register;

a performance monitoring unit; and

one or more hardware counters located within the performance monitoring unit; wherein the one or more hardware counters count events that occur during processing of the interrupt responsive to the interrupt unit determining that the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt unit control register.

8. A method of executing instructions in a data processing system, comprising:

receiving a signal at a microprocessor of the data processing system for invoking an interrupt, wherein the interrupt includes a plurality of states; and

counting at least one event for a selected state of the plurality of states during processing of the interrupt.

Prior Art

Levine	5,691,920	Nov. 25, 1997

M. Morris Mano, *Computer System Architecture*, pp. 434-443 (Prentice-Hall, 2nd ed. 1982) ("Mano").

Examiner's Rejections

Claims 1-7 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite.

Claims 1-7 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement.

Claims 16 and 23 stand rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter.

Claims 1-6, 8-12, and 16-21 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Levine.

Claims 1-6, 8-14, and 16-21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the admitted prior art (Spec. page 3, final paragraph) and Levine.

Claims 7, 15, and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Levine and Mano or over the admitted prior art, Levine, and Mano.

ANALYSIS

Claims 1-7 -- Section 112, second paragraph

The Examiner considers claim 1 to be indefinite because relationships between the elements are not specified. Appellants respond that the inter-relationship of the components is set forth in the final portion of the claim. Appellants also refer to instant Figure 5 and the Specification at page 21, line 17 through page 22, line 2 and page 25, line 28 through page 27, line 6 as "support" for how the claim is to be interpreted.

However, as described in the Specification at the indicated sections, and in the Appeal Brief's (at 6) "Summary of Claimed Subject Matter," the "interrupt control register" 308 (Fig. 3) is part of "interrupt unit" 304. Yet, claim 1 recites the "interrupt unit control register" and the "interrupt unit" as separate elements. The claim thus contains a latent ambiguity.

While the scope of claim 1 might be reasonably clear when read "in a vacuum," when the terms are interpreted in light of the Specification, as they must, a latent ambiguity renders the scope of the claim indeterminate. *See In re Moore*, 439 F.2d 1232, 1255 n.2 (CCPA 1971) (discussing latent ambiguity in claims).

We therefore sustain the rejection of claim 1, and that of claims 2 through 7 which depend from claim 1, under 35 U.S.C. § 112, second paragraph.

Claims 1-7 -- Section 112, first paragraph

The Examiner finds that the disclosure does not provide written description support for the claim 1 feature that the one or more hardware counters count events that occur during processing of the interrupt "responsive to the interrupt unit determining that the interrupt is of the interrupt type selected to be monitored as indicated by the interrupt control register."

However, the disclosure appears to provide adequate written description support for what happens "responsive to" the interrupt unit determination, in view of Appellants' reliance (App. Br. 10-11) on Figure 5 and text at pages 21, 22, and 25 through 27 of the Specification. We do not find any satisfactory explanation from the Examiner in support of why the disclosure is deemed to lack written description support for the claim language pointed out by the rejection.

We thus do not sustain the § 112, first paragraph rejection of claims 1-7.

Claims 16 and 23 -- Section 101

Claims 16 and 23 are rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter.

Appellants' Notice of Appeal (filed Feb. 29, 2008) states that appeal is taken from the Final Office Action (Final Rejection) finally rejecting "claims 1-23." The § 101 rejection was the only ground of rejection entered against claim 23 in the Final Rejection.

With respect to the § 101 rejection, the Appeal Brief (at 8) states that "Appellants are not appealing this rejection" and "Appellants agree to amend the claims as necessary at the appropriate time."

Appellants do not tell us what might be an "appropriate time." Appellants did not amend or cancel claims 16 and 23 contemporaneous with, or subsequent to, the Notice of Appeal.

Claims 16 and 23 are before us. The § 101 rejection is also before us, as the Examiner has not withdrawn the rejection but repeats it in the Answer.

In view of Appellants' failure to contest the merits of the rejection, we summarily sustain the § 101 rejection of claims 16 and 23.[2]

Claims 1-22 -- Sections 102 and 103(a)

The Examiner finds that at least bits 5 and 16, as shown in Figure 6A of Levine, indicate "an interrupt type selected to be monitored" as recited in claim 1.

Levine teaches that bits 5, 16, and 17 in the "Monitor Mode Control Register" depicted in Figure 6A are used to control interrupt signals, rather than to distinguish between types of interrupts. *See* Levine col. 11, ll. 46-47.

We agree with Appellants that the rejections applied against claim 1 do not identify any teaching in Levine of an interrupt unit control register that indicates an interrupt *type* selected to be monitored, as claimed.

[2] The Examiner does not indicate why dependent claims 17-22, drawn to the "computer program product" of claim 16, are not also rejected under § 101.

Instant claim 8 recites counting events "during processing of the interrupt." Instant claim 16 recites counting at least one event "during processing of the interrupt."

We agree with Appellants that the rejections applied against claims 8 and 16 fail to identify any teaching in Levine of counting events during processing of an interrupt. On the contrary, the reference appears to teach that the counters identified in the rejections -- PMCs 51 (Fig. 4) -- count events that occur prior to, and consequently can initiate, the interrupts. *See, e.g.,* Levine col. 10, l. 57 - col. 11, l. 19; col. 11, ll. 46-47.

Claims 1, 8, and 16 are the independent claims rejected over the prior art. Because the rejections under §§ 102 and 103(a) rely on the asserted teachings of Levine that we find to be deficient on this record, we do not sustain any of the rejections over the applied prior art.

DECISION

The rejection of claims 1-7 under 35 U.S.C. § 112, second paragraph, as being indefinite is affirmed.

The rejection of claims 1-7 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement is reversed.

The rejection of claims 16 and 23 under 35 U.S.C. § 101 as being directed to non-statutory subject matter is affirmed.

The rejections of claims 1-22 under 35 U.S.C. §§ 102 and 103(a) are reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). *See* 37 C.F.R. § 41.50(f).

AFFIRMED-IN-PART

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